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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,063	12/09/2003	Anand Rajagopalan	NVDA P000785	3734
26291 7590 05/17/2007 PATTERSON & SHERIDAN L.L.P. 595 SHREWSBURY AVE, STE 100 FIRST FLOOR SHREWSBURY, NJ 07702			EXAMINER VIDWAN, JASJIT S	
			ART UNIT 2182	PAPER NUMBER
			MAIL DATE 05/17/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/731,063

Applicant(s)

RAJAGOPALAN ET AL.

Examiner

Jasjit S. Vidwan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 15 February 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-6, 8-10, 21, 22 and 24-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6, 8-10, 21, 22 and 24-28 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 2/19/2007.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application
- ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/15/2007 has been entered.

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, & 10 rejected under 35 U.S.C. 102(b) as being anticipated by Boucher et al U.S. Patent No: 6,334,153 **[herein after Boucher]**.

3. **As per claims 1**, Boucher teaches a system for uploading frame data to system memory, the system comprising:

(a) CPU coupled to the system memory and configured to execute an application program **[Col. 5, Lines 10-24]**.

(b) CPU executing a Transmission Control Protocol (TCP) stack which includes code to complete at least some TCP processing **[Col. 6, Lines 22-38]**

(c) Hardware subsystem preconfigured to process all frames related to one or more connections delegated by the TCP stack to produce frame data **[Col. 2, Lines 60-67, "processing bits of incoming network data"]** and upload the frame data to a portion of system memory allocated to the application program **[Col. 3, Lines 56-62, The Fast-path method delivers data directly to intended destination which is the Application Program]**

(d) System memory including a connection table (CT) storing data for all active connections with system including delegated connections [Col. 45, Lines 16-28], reads and writes to the CT being made directly through the hardware [Col. 4, Lines 6-10]

(e) Hardware subsystem being further preconfigured to request legacy processing by the TCP stack of the frames of the delegated connections [Col. 6, Lines 54-56]

4. **As per Claim 10**, Boucher as modified by Adams teaches a method of uploading frame data including Transmission Control Protocol (TCP) payload data [Col. 6, Lines 22-38] to system memory, the method comprising

(a) Processing a frame to produce frame data [Col. 2, Lines 60-67, *"processing bits of incoming network data"*]

(b) Uploading the frame data to either a portion of system memory comprising a user buffer allocated to an application program [Col. 3, Lines 56-62, *The Fast-path method delivers data directly to intended destination which is the Application Program*] or a legacy buffer in the system memory for separate TCP processing by a TCP stack executing on a CPU depending on whether the user buffer is available [Col. 2, Lines 44-59, *The slow-path method adds headers of each layer prior to sending the frame to the second host*]

5. (c) Utilizing hardware separate from the CPU which does the TCP processing] to partially process the frame and determine whether the frame was delegated by the separate TCP processing [Col. 4, Lines 6-10, *"The specialized microprocessor and the host intelligently choose whether a given message or portion of a message (partially processed frame) is processed by the microprocessor (hardware) or the host stock (software)"*]

6. **As per claims 2**, Boucher teaches a system wherein the frame data is payload data [Col. 2, Lines 60-67, *data without headers*]

7. **As per claims 3**, Boucher teaches a system wherein a TCP Stack [Col. 6, Lines 22-38, *data handled by TCP protocols, therefore TCP stack handles fast-path data*] provides the hardware with a physical address corresponding to a user buffer [Col. 18, Lines 61-63]

8. **As per claim 13**, Boucher teaches a system wherein the portion of system memory is a user buffer [Col. 3, Lines 56-62].

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 4-6, 8-9, 21-22, 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher and further in view of Adams, U.S. Patent No: 6,775,693 [herein after Adams].

11. **As per claims 4, 5 and 6**, Boucher teaches the limitations of claims 1 and 10. Boucher further teaches a method for slow-path processing which is the conventional method of transferring and processing data where the frame data is moved to a secondary storage prior to being processed by the Host. However, Boucher does not explicitly teach system wherein the hardware is configured to process frames to produce partially processed frame data and further uploading the partially processed frame data to a portion of system memory allocated to a software driver. However, Adams teaches a system wherein the hardware is configured to process frames to produce partially processed frame data and further uploading the partially processed frame data to a portion of system memory allocated to a software driver [See Adams, Col. 8, Lines 38-45].

It would have been obvious for one of ordinary skill in the art at the time of Applicant's invention to combine the teachings of Boucher with that of Adams in order to take advantage of having a dual option for the microprocessor and the host to intelligently choose whether a given message or portion of a message is processed by fast-path or slow-path [Col. 4, Lines 5-10]. It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the two teachings in order to take advantage of having a dual option for the microprocessor and the host to

intelligently choose whether a given message or portion of a message is processed by fast-path or slow-path [Col. 4, Lines 5-10].

12. **As per claims 8**, teachings of Boucher as modified by Adams teach a system wherein a software driver provides the hardware with a tag corresponding to a location of the legacy buffer [See Adams, Col. 8, Lines 46-51]

13. **As per claim 9**, teachings of Boucher as modified by Adams teach a system wherein the hardware is configured to transmit the tag to the software driver [See Adams, Col. 8, Lines 38-45].

14. **As per Claim 21**, teachings of Boucher as modified by Adams teach a system wherein the hardware is configured to pause incoming frame data to determine whether a frame is invalid, the invalid frame being stored in the legacy buffer for legacy processing [Col. 58, Lines 9-29].

15. **As per Claim 22**, teachings of Boucher as modified by Adams teach a system wherein the TCP stack is configured to process the frame data up loaded to the legacy buffer by the hardware [Col. 2, Lines 44-59]

16. **As per Claim 24**, teachings of Boucher as modified by Adams teach a method wherein the TCP stack completes processing of the partially processed frame stored in the legacy buffer [Fig. 4, element 62, "Cache"].

17. **As per Claim 25**, teachings of Boucher as modified by Adams teaches a method wherein the partial processing of the frame produces partially processed frame and header data [See Adams, Col. 8, Lines 38-45]

18. **As per Claim 26**, teachings of Boucher as modified by Adams teach a method wherein the user buffer is defined as not available when the processed frame portion exceeds a start up limit value associated with the delegated connection carrying the frame being processed [Col. 2, Lines 60 – Col. 3, Line 5]

19. **As per Claim 27**, teachings of Boucher as modified by Adams teach a method wherein the uploaded frame data includes TCP payload data [Col. 6, Lines 22-38]

20. **As per Claim 28**, teachings of Boucher as modified by Adams teach a system wherein the hardware accesses the CT using the distribution port field of a frame as a direct index into the CT **[Col. 6, Line 66 - Col. 7, Line 15]**

***Response to Arguments***

21. Applicant's arguments filed 02/19/2007 have been fully considered but they are not persuasive. Applicant argues that as amended, prior art of record fails to teach limitation of "...reads and writes to the CT being made directly through the hardware". Further, Applicant argues that as amended, the claim language overcomes Examiner provided Boucher citation that states "...specialized microprocessor and the host (both hardware) intelligently choose whether a given message or portion of a message is processed by the microprocessor (hardware) or the host stack (software)."

22. With respect to Applicant's argument, **Examiner disagrees**. Applicant's argument is based on an argument that Boucher "chooses" whether to process certain data via either hardware or software, whereas Applicant's invention permanently separates hardware tasks from that of software. Applicant asserts that this limitation is evident by Applicant's amendment to read "hardware subsystem **preconfigured** to process all frames to process all frames related to one or more connections delegated by the TCP stack." It should be noted that Boucher teaches a system having two separate data transfer methods; Fast-path (handled by hardware without need for headers) and slow-path (handled by software with the use of headers) **[see Col. 3, Lines 56 Col. 4, Line 10]**. The distinction between which method the transfer will take place is predetermined by the type of data transfer requested **[Col. 6, Lines 22-38]**. More importantly, Boucher attempts to transfer majority of the messages via fast-path method (through the use of hardware) with only "small portions" of frames left for conventional software based transfer **[see Col. 6, Lines 43-56]**. The above method is similar to that of Applicant's own invention wherein as recited in the claim language itself, "the hardware subsystem being further preconfigured to request legacy processing (software based) by the TCP stack of the frames of the delegated connections." In other words, the hardware subsystem is configured to handle message requests via hardware only, however is capable of transferring the data via software as well if needed. Likewise,

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Boucher's system has a predetermined distinction on type of data that would qualify for fast-path, however is capable of using legacy transfer for those messages that do not qualify for predetermined protocols for fast-path transfer. Therefore, in light of the above argument, Examiner submits that prior art of record still reads on Applicant's claimed invention.


**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM HUYNH can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV  
5/8/07

  
KIM HUYNH  
SUPERVISORY PATENT EXAMINER  
5/14/07